

REMARKS

Applicant respectfully requests reconsideration of this application as amended.
Claim 1 is amended. Claims 27-127 are added.

Applicant would like to take this opportunity to discuss added Claims 32-33, 34-35, 40-42, and 45-46.

For the Examiner's reference, copies are attached hereto of an Appeal Brief in the case of Application No. 08/522,067 (the parent application) and of a Decision on Appeal No. 1998-0524 from the final rejection of Claims 24-26 and 28-33 in the parent application (the art relied upon being: Ando et al., US Pat. No. 4,771,379; and Shipnes, J. "Graphics Processing with the 88110 RISC Microprocessor," 1992, pp. 169-174).

Applicant wishes to point out that Claims 32 and 33 in the present application are derived from Claims 24 and 29, respectively, in the parent application; that Claims 34 and 35 in the present application are derived from Claims 25 and 30, respectively, in the parent application; that Claims 40, 41 and 42 in the present application are derived from Claims 26, 31 and 32, respectively, in the parent application; and finally that Claims 45 and 46 in the present application are derived from Claims 28 and 33, respectively, in the parent application. On August 11, 2000, prior to receiving the Decision on Appeal No. 1998-0524, Applicant requested the appeal be withdrawn and amended the claims in the parent application.

Since the patentability of the original Claims 24-26 and 28-33 over the references cited is supported by the Decision on Appeal in the parent application, Applicant believes Claims 32-33, 34-35, 40-42, and 45-46, as well as Claims 36, 43-44, and 47, which are dependent therefrom in the present application, are in condition for allowance.

Some minor changes have been made to the original claims of the parent application, such as the removal of phrases, "the steps of" and "in a computer system," from preambles of certain claims. These changes have been made to impart precision to

the claims, rather than to avoid prior art. Applicant does not believe the changes affect patentability of Claims 32-33, 34-35, 40-42, and 45-46 in the present application.

In addition, Applicant would also like to take this opportunity to direct the Examiner's attention to art submitted on November 19, 2001, which may be considered pertinent to Applicant's disclosure:

Murakami et al., US Pat. No. 5,442,799;

Ulrich, US Pat. No. 5,111,422; and

Nakamura, US Pat. No. 5,457,805.

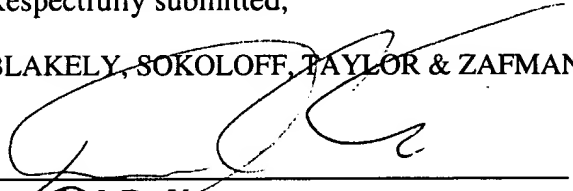
Applicant respectfully solicits the Examiner to grant allowance of the pending Claim 1 as amended and the added Claims 27-127.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 2/19, 2002


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VERSION OF SPECIFICATION AND CLAIMS WITH MARKINGS:

IN THE SPECIFICATION

The paragraph beginning on page 1, line 6 is amended:

[Serial. No. __, titled "A Method and Apparatus for Performing Multiply-Subtract Operations on Packed Data," filed _____, by Alexander D. Peleg, Millind Mittal, Larry M. Mennemeier, Benny Eitan, Andrew F. Glew, Carole Dulong, Eiichi Kowashi, and Wolf Witt.] Continuation of application Ser. No. 08/522,067, filed August 31, 1995, pending. Application No. 08/960,413, titled "Apparatus for Performing Multiply-Add Operations on Packed Data," filed Oct. 29, 1997, now Pat. No. 5,983,256, which is a Continuation of Ser. No. 08/551,196, filed Oct. 31, 1995, abandoned, which is a Continuation of Ser. No. 08/522,067, filed August 31, 1995, pending. Application No. 606,212, titled "Apparatus for Performing Multiply-Add Operations on Packed Data," filed Feb 23, 1996, now Pat. No. 6,035,316, which is a CIP of Ser. No. 08/522,067, filed August 31, 1995, pending. Application No. 554,625, titled "An Apparatus for Performing Multiply-Subtract Operations on Packed Data," filed November 6, 1995, now Pat. No. 5,721,892, which is a Continuation of Ser. No. 521,803, filed Aug. 31, 1995, abandoned.

The paragraph beginning on page 4, line 15 is amended:

Another prior art DSP includes a multiply accumulate instruction that operates on two sets of two values and an accumulation value (See "Digital Signal Processor with Parallel Multipliers", patent number 4,771,[470]379- referred to herein as the "Ando et al." reference). An example of the multiply accumulate instruction for this DSP is shown below in Table 2, where the instruction is performed on the data values A₁, A₂, B₁ and B₂ accessed as Source1-4, respectively.

The paragraph beginning on page 15, line 10 is amended:

Execution unit 130 is used for executing instructions received by processor 109. In addition to recognizing instructions typically implemented in general purpose processors, execution unit 130 recognizes instructions in packed instruction set 140 for performing operations on packed data formats. Packed instruction set 140 includes instructions for supporting multiply-add and/or multiply-subtract operations. In addition, packed instruction set 140 may also include instructions for supporting a pack operation, an unpack operation, a packed add operation, a packed subtract operation, a packed multiply operation, a packed shift operation, a packed compare operation, a population count operation, and a set of packed logical operations (including packed AND, packed ANDNOT, packed OR, and packed XOR) as described in "A Set of Instructions for Operating on Packed Data ," filed on [_____, serial number _____] Aug. 31, 1995, application number 521,360.

The paragraph beginning on page 31, line 20 is amended:

In contrast, the disclosed multiply-add and multiply-subtract instructions do not carry forward an accumulation value. As a result, these instructions are easier to use in a wider variety of algorithms. In addition, software pipelining can be used to achieve comparable throughput. To illustrate the versatility of the multiply-add instruction, several example multimedia algorithms are described below. Some of these multimedia algorithms use additional packed data instructions. The operation of these additional packed data instructions are shown in relation to the described algorithms. For a further description of these packed data instructions, see "A Set of Instructions for Operating on Packed Data," filed on [_____, serial number _____] Aug. 31, 1995,

application number 521,360. Of course, other packed data instructions could be used. In addition, a number of steps requiring the use of general purpose processor instructions to manage data movement, looping, and conditional branching have been omitted in the following examples.

Table 6a on page 32 is amended:

Multiply-Add Source1, Source2				
r1	i[2]1	r1	i1	Source1
r2	-i2	i2	r2	Source2
=				
Real Component: $r1r2-i1i2$		Imaginary Component: $r1i2+r2i1$		Result 1

Table 6a

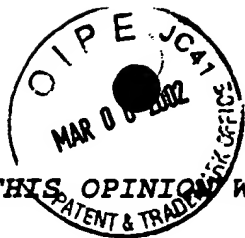
IN THE CLAIMS

Claim 1 is amended:

- (Amended once) An apparatus for use in a computer system comprising:
 - a memory having stored therein a first packed data comprising at least four data elements and a second packed data comprising at least four data elements; and
 - a processor coupled to said memory to receive said first packed data and said second packed data, said processor performing operations on data elements in said first packed data and said second packed data to generate a plurality of data elements in a third packed data in response to receiving an instruction, at least two of said plurality of data elements in said third packed data storing the result of multiply-add operations.

New claims 27-127 are added.

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THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

MAILED

Paper No. 16

AUG 29 2000

UNITED STATES PATENT AND TRADEMARK OFFICE

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AND INTERFERENCES

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALEXANDER D. PELEG, MILLIND MITTAL, LARRY M. MENNEMEIER,
BENNY EITAN, CAROLE DULONG, EIICHI KOWASHI and WOLF WITT

Appeal No. 1998-0524
Application No. 08/522,067

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ON BRIEF

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
LOS ANGELES

Before JERRY SMITH, BARRETT and HECKER, *Administrative Patent Judges*.

HECKER, *Administrative Patent Judge*.

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U.S. PAT. & TRADEMARK OFFICE

DATA PROCESSING DEPT.
Jc

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 24 through 26 and 28 through 33, all claims pending in this application.

The invention relates generally to the field of computer systems, and in particular, the area of packed data instructions. In typical computer systems, processors are implemented to operate on values represented by a large number of bits (e.g., 64) using instructions that produce one result. However, some

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applications require the manipulation of large amounts of data which may be represented in a small number of bits (e.g., in multimedia applications). To improve efficiency in such applications, certain processors provide packed data formats. A packed data format is one in which the bits typically used to represent a single value are broken into a number of fixed sized data elements, each of which represents a separate value. For example, a 64-bit register may be broken into two 32-bit elements, each of which represents a separate 32-bit value. Prior art processors provide instructions for separately manipulating each element in these packed data types in parallel. For example, a packed add instruction independently adds together corresponding data elements from a first packed data and a second packed data. Thus, if a multimedia algorithm requires a loop containing five operations that must be performed on a large number of data elements, it is desirable to pack the data and perform these operations in parallel using packed data instructions. In this manner, these processors can more efficiently process multimedia applications.

With reference to the claimed invention, execution of a single packed data instruction causes at least two independent

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multiply-add operations on packed data inputs. See for example, Table 3a in Appellants' specification.

Representative independent claim 28 is reproduced as follows:

28. In a computer system, a method for manipulating a first packed data and a second packed data responsive to the execution of a single instruction, said first packed data including A_1, A_2, A_3 , and A_4 as data elements, said second packed data including B_1, B_2, B_3 , and B_4 as data elements, said method comprising the steps of:

 multiplying together A_1 [sic] and B_1 [sic] to generate a first intermediate result;

 multiplying together A_2 [sic] and B_2 [sic] to generate a second intermediate result;

 multiplying together A_3 [sic] and B_3 [sic] to generate a third intermediate result; and

 multiplying together A_4 [sic] and B_4 [sic] to generate a fourth intermediate result;

 performing in parallel the following steps:

 adding together said first intermediate result and said second intermediate result to generate a first data element in a third packed data; and

 adding together said third intermediate result and said fourth intermediate result to generate a second data element in said third packed data; and

 saving said third packed data for use as an operand to another instruction.

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The Examiner relies on the following references:

Ando et al. 4,771,379 Sep. 13, 1988

Shipnes, "Graphics Processing with the 88110 RISC
Microprocessor," IEEE, 1992, pp. 169-174.

Claims 24 through 26 and 28 through 33 stand rejected under
35 U.S.C. § 103(a) as being unpatentable over Ando in view of
Shipnes.

Rather than reiterate the arguments of Appellants and the
Examiner, reference is made to the brief and answer for the
respective details thereof.

OPINION

After a careful review of the evidence before us, we will
not sustain the rejection of claims 24 through 26 and 28 through
33 under 35 U.S.C. § 103.

The Examiner has failed to set forth a **prima facie** case. It
is the burden of the Examiner to establish why one having
ordinary skill in the art would have been led to the claimed
invention by the reasonable teachings or suggestions found in the
prior art, or by a reasonable inference to the artisan contained
in such teachings or suggestions. **In re Sernaker**, 702 F.2d 989,
995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when .

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determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (*citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984)).

The Examiner indicates that Ando teaches the claimed invention except for explicitly disclosing the technique of performing the operations on packed data. However, since it is well known to use packed data formats to improve efficiency, as evidenced by Shipnes, the Examiner concludes that it would have been obvious to have used a packed data format in Ando to more efficiently process data, e.g., multimedia data. (Final rejection, paper no. 9 and paper no. 7.)

Appellants argue that their single instruction operation requires a multiply-add operation, **without** accumulation. The Ando-Shipnes combination **always** sums the results **of all** of the multiplications and adds **a previously stored accumulation value** to generate a **single** result value (brief-page 5). Appellants state:

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Each of Applicant's independent claims requires either:
1) that execution of the instruction is completed **without summing/accumulating** the results of the multiply-add operations and without **adding an accumulation value** (claim 24 -"without adding said first and second data elements"; and claim 26 -"without summing said plurality of result data elements"); or
2) that a packed result containing the two **unaccumulated** data elements is stored as an operand for use by another instruction (claims 25 and 28). (Brief-pages 6 and 7.)

Appellants note that zeroing the accumulation value of the Ando-Shipnes combination would be costly and inefficient (brief-page 7).

The Examiner responds that **when** the accumulation value is **zero**, the Ando-Shipnes combination provides the same result. (Answer-page 5.)

We find that this explanation falls short of teaching the claimed invention. The supposition that one set of isolated circumstances would produce the same result is unconvincing. The fact that accumulation occurs at all, is contrary to the claimed invention, as argued by Appellants.

The Examiner responds further, with respect to zeroing the accumulation value:

[S]ince the results of multiplications (e.g., $A1*B1$, $A2*B2$) of the data elements (e.g., $A1$, $B1$, $A2$, and $B2$) are for a certain period of time available in the accumulator before any addition (accumulation) can be

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performed, one of ordinary skill in the art, if it were considered desirable for any reason to just store the results of multiplications without adding them, would have implemented the claimed invention. (Answer-pages 5 and 6.)

We take the Examiner's response to mean that any computer programmer is capable of writing a computer instruction to multiply-add, **without** accumulation, depending on the desired calculations pertaining to the algorithm being implemented. We might be convinced that such an instruction is considered to be within the skill of the typical programmer if there were some evidence of such in this record. In the absence of such evidence, we cannot support the Examiner's position.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." **In re Fritch**, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), **citing In re Gordon**, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." **Para-Ordnance Mfg. v. SGS Importers Int'l**, 73 F.3d at

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1087, 37 USPQ2d at 1239, *citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

As pointed out above, the Examiner's rejection lacks motivation to remove the accumulator from Ando. Shipnes does not cure the deficiencies of Ando. Shipnes was merely relied upon to teach the use of the packed data format. This is not disputed by Appellants.

Thus, in view of the above, we will not sustain the Examiner's rejection of independent claims 24, 25, 26 and 28.

The remaining claims on appeal also contain the above limitations discussed in regard to the independent claims, and thereby we will not sustain the rejection as to these claims.

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We have not sustained the rejection of claims 24 through 26 and 28 through 33 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

Gerry Smith
JERRY SMITH

JERRY SMITH
Administrative Patent Judge

Lee E Barrett
LEE E. BARRETT

LEE E. BARRETT
Administrative Patent Judge

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STUART N. HECKER
Administrative Patent Judge

Appeal No. 1998-0524
Application No. 08/522,067

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